IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

Claims 1-6 (canceled)

7. (Original) A system for transparently transporting data comprising:

an ingress module configured to convert a first data stream to an second data stream, wherein the ingress module comprises

an ingress buffer configured to store the first data stream,

an ingress counter configured to count the bits of the first data stream which are stored in the ingress buffer,

an ingress timer, and

write logic coupled to the ingress counter and the ingress timer and configured to determine the data rate of the first data stream, wherein the write logic is further configured to periodically write the data rate of the first data stream into the ingress buffer;

an egress module configured to receive the second data stream and to convert the second data stream to a third data stream, wherein the egress module is configured to reproduce the bit sequence and timing of the first data stream in the third data stream,

wherein the egress module comprises

an egress buffer configured to store the second data stream,

a phase locked loop (PLL) configured to control the rate at which data is read out of the egress buffer to produce the third data stream,

an egress counter configured to count the bits of the third data stream,

timing logic coupled to the egress counter and the egress timer and configured to determine the data rate of the third data stream and to control the PLL to match the data rate of the third data stream to the data rate of the first data stream; and

a transport medium coupled between the ingress module and the egress module and configured to convey the second data stream from the ingress module to the egress module.

8. (Original) The system of claim 7 wherein the timing logic is configured to determine a difference between the data rate of the first data stream and the data rate of the third data stream, and wherein the timing logic is configured to increase the frequency of the PLL if the data rate of the first data stream is greater than the data rate of the third data stream and to decrease the frequency of the PLL if the data rate of the first data stream is less than the data rate of the third data stream.

9. (Original) The system of claim 7 wherein the ingress module is configured to transmit a clock signal with the second data stream, wherein the ingress module is configured to determine the data rate of the first data stream based upon the clock signal, and wherein the egress module is configured to determine the data rate of the third data stream based upon the clock signal.

10. (Original) The system of claim 7 wherein the first data stream is an optical data stream, the second data stream is an electrical data stream, and the third data stream is an optical data stream, wherein the ingress module further comprises an optical-to-electrical converter and wherein the egress module further comprises an electrical-to-optical converter.

Claims 11-31 (canceled)

32. (Currently amended) A system for transparently transporting optical data over a electrical medium comprising:

an ingress module configured to convert a first optical data stream to an electrical data stream;

an egress module configured to receive the electrical data stream and to convert the electrical data stream to a second optical data stream;

wherein the egress module is configured to reproduce the bit sequence and timing of the first optical data stream in the second optical data stream.;

wherein the egress module comprises a buffer configured to store the electrical data stream, a phase locked loop (PLL) configured to control the rate at which data is read out of the buffer, a counter configured to count the bits of the data stream which are read out of the buffer, and an electrical-optical converter configured to convert the bits of the data stream which are read out of the buffer to the second optical data stream;

timing logic coupled to the counter and configured to determine the number of bits of the data stream which are read out of the buffer during each of a second plurality of regular intervals; and ~~The system of claim 31~~

wherein the timing logic is coupled to the PLL, wherein the timing logic is configured to determine a difference between the number of bits of the data stream which are stored in the buffer during one of the intervals and the number of bits of the data stream which are read out of the buffer during one of the intervals, and wherein the timing logic is configured to increase the frequency of the PLL if the number of bits of the data stream which are stored in the buffer is greater than the number of bits of the data stream which are read out of the buffer and to decrease the frequency of the PLL if the number of bits of the data stream which are stored in the buffer is less than the number of bits of the data stream which are read out of the buffer.

Claims 33-35 (Canceled)